ABSTRACT OF THE DISCLOSURE

A three-dimensional model of a semiconductor chip is produced from coarsely aligned mosaic images of respective layers of the semiconductor chip using an improved method for aligning the mosaic images, so that minimal operator intervention is required to produce the model. A line detection algorithm is applied to each of the mosaic images to produce a set of line segments identified by x and y coordinates of end points of the line segments with respect to a frame defined by a mosaic image in which each line segment occurs. Virtual reference marks are established using end points of different mosaic images that are vertically aligned to within an uncertainty of the coarse alignment of the mosaic images, and the virtual reference marks are used to compute a mean adjustment of the x and y coordinates of each of the mosaic images to produce a three dimensional coordinate space. The end points are processed within the three dimensional coordinate space to define vias, lines and branch lines of the semiconductor chip, which are used to build the three-dimensional model. Operator intervention is only required to verify putative line segments that are marked as uncertain because of poor agreement with predefined rules. The 3-D model may be annotated and viewed separately from the mosaic images.